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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,800	06/28/2001	Michael J. Peterson	S01.12-0746/STL 9879	7097

7590 09/16/2003

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EXAMINER

PATEL, ISHWARBHAI B

ART UNIT PAPER NUMBER

2827

DATE MAILED: 09/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary**Application No.**

09/893,800

Applicant(s)

PETERSON ET AL.

Examiner

Ishwar (I. B.) Patel

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 January 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 15 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 and 16-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 January 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims 1-14 and 16-20 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Drawings

2. The drawings were received on January 7, 2003. These drawings are approved.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Kato et al., US Patent No. 4,823,217, hereafter, Kato.

Regarding claim 1, Kato discloses an apparatus comprising:

a connection pad and a trace operably disposed on an operating surface of the flex circuit substrate, the trace being adjacently and operably connected to the

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connection pad (flexible printed circuit board 17 having conductor pattern 18, see figure 3, column 6, line 11-20); and

a barrier that crosses the trace and is configured to limit a flow of material down the trace (protective stripes 20 and 21, see figure 3, column 6, line 11-20).

Regarding claim 2, Kato further discloses the barrier spaced from the connection pad, see figure 3.

5. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato, as applied to claims 1 and 2 above.

Regarding claim 3, 4 and 5, the applicant is claiming the distance between the pad and the barrier as less than half the diameter of the connection pad as claimed in claim 3 and that between a range of one half to two times the diameter of the connection pad, as claimed in claim 5 and the barrier contact the connection pad, as claimed in claim 4.

Kato discloses the protective stripes adjacent and extremely close to the connecting 18A and 18B, see figure 3, column 6, line 24-26.

Further, the distance will depend upon many variables such as the quantity of solder material used, size of the pad, width of the connecting traces, additional solder coating is provided on the pads in advance or not, in certain application partial covering of the pad is advisable and in certain application the pads are kept completely open to

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have solder connection on the side of the pads and a person of ordinary skill in the art will select the configuration to have reliable solder connection for specific applications.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide circuit structure of Kato with the spacing between the barrier and the connection pad as claimed in claims 3, 4 and 5, in order to have reliable solder connection for the specific applications.

6. Claims 6-9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato, as applied to claims 1-5 above, and further in view of Shirasaki et al., US Patent No. 5,378,859, hereafter, Shirasaki, Yoneda, US Patent No. 6,049,122 and Kondo et al., US Patent No. 6,303,878, Kusui, US Patent No. 6,441,316.

Regarding claims 6-9 and 13, the applicant is claiming a cover layer which substantially cover the operating surface of the flex circuit substrate and the barrier layer formed by selectively depositing the cover layer as claimed in claim 6, the connection pad exposed, free of the cover layer, as claimed in claim 7, the connection pad and the portion of the trace proximate the connection pads are exposed, free of cover layer, as claimed in claim 8, a length between the connection pad and the barrier is exposed and free of the cover layer and the barrier is formed by the cover layer, as claimed in claim 9 and connection pad and a length of the trace proximate the connection pad are located within the cover layer open area, as claimed in claim 13.

Kato fails to disclose the cover layer substantially covering the operating surface of the operating substrate.

Shirasaki discloses a cover layer 25 covering the operating surface of the film wiring board except the semiconductor connecting are including the pads and the connecting traces near the pads, see figure 1A and 1B and even covering the area below the semiconductor device 24, see figure 3C.

Yoneda discloses covering the operating surface substantially except the contact area with pad and connecting traces, see figure 3.

Kondo discloses a mounting structure with operating surface covered by a solder resist exposing the dummy pads and connection pads, see figure 1-4.

Kusui discloses a protection layer exposing traces connected to the pad in order to facilitate testing to confirm the reliable solder flow.

A person of ordinary skill in the art will decide depending upon the specific application, how much covering is to be applied to have the desired protection of the surfaces. Also, it will be advantageous to provide the barrier layer formed of the same cover layer to save labor, time and material cost as it can be applied at the same time when the cover layer is applied.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the barrier stripes and the cover layer as claimed in claim 6-9 and 13, as per the teaching of Shirasaki, Yoneda and Kondo in order to have desired covering of the surface for the protection and reliable connection structure.

Regarding claims 11 and 12, Kato discloses the protective film is formed by resist, column 6, line 38-40. Though, Kato does not explicitly disclose the type of resist, both dry film solder mask, as claimed in claim 11, and liquid photoimageable solder mask, as claimed in claim 12, are well known in the art and a person of ordinary skill will use any of the resist to have desired protection for the specific application.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the barrier stripes of Kato made of dry film solder mask or liquid photoimageable solder mask, as claimed in claims 11 and 12, in order to have the solder stop for reliable connection structure.

Regarding claim 14, the combinations structure of Kato, Shirasaki, Yoneda and Kondo discloses all the features of the claimed invention including the dummy pad, as applied to claim 6-9 above.

Regarding claim 16-20, the combinations structure of Kato, Shirasaki, Yoneda and Kondo discloses all the features of the claimed invention including the flex circuit substrate and the barrier strip which will stop the solder reflow, as applied to claim 1 and 6-9 above and a non operational pads, as applied to claim 14 above.

Response to Arguments

7. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

The new prior art of Kato discloses the barrier strip on a flex substrate. Further, these are the structural claims and the exact function of the elements in the prior art may be different than that claimed by applicant, however the solder stop or barrier strip stopping the solder flow will inherently help in maintaining the gap between the device or the carrier and the circuit board.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Isenberg et al. discloses a solder stop for electrical connection.

Myers et al., discloses solder stop for electrical connector.

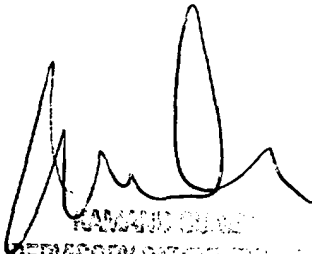
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (703) 305 2617. The examiner can normally be reached on M-F (8:30 - 5).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703) 308 1233. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305 3900.

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lbp
9/7/03


KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY DIVISION